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Impact of Band Structure on Phonon-Limited Electron Mobility Behavior of Germanium-on-Insulator Layer with (001) and (111) Surfaces

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***Abstract*—** This paper studies the phonon-limited electron mobility of the inversion layer at room temperature for ultra-thin body (001) Ge and (111) Ge layers in single-gate (SG) and double-gate (DG) germanium-on-insulator (GOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) aiming at future radio-frequency applications. Simulations are based on one-dimensional self-consistent calculations and relaxation time approximations. Assuming a 7.2-nm-thick GOI layer on (001) Ge surface, it has been demonstrated that intra-valley phonon scattering in the DG GOI MOSFET inversion layer is strongly suppressed within a range of medium and high effective field values; DG GOI MOSFETs have higher phonon-limited electron mobility than SG GOI MOSFETs. The suppression of intra-valley-phonon scattering in a 7.2-nm-thick DG GOI MOSFET primarily stems from the reduction in the form factor at medium and high effective field values. However, it is shown that the use of the (001) Ge surface offers little merit in DG GOI MOSFETs because the mobility value is not large. It is demonstrated that the superior electron mobility on the (111) Ge surface of SG GOI MOSFETs confirms the significant merit of this structure with regard to applications because acoustic-phonon scattering events are significantly reduced in the non-degenerate *L* valley. Primary mechanism responsible for this fact is that some inter-subband form factors of electrons sharing the lowest subband of the non-degenerate *L* valley decrease at low effective field values, while the intra-subband form factor of electrons sharing the lowest subband of the non-degenerate *L* valley remains large. The expected phonon-limited electron mobility of SG GOI MOSFETs having a 4-nm-thick GOI layer, for example, with (111) Ge surface, is about 2300 $cm^2/V/s$ at the effective field of 0.5 MV/cm; this is about 400% of that of the equivalent SG GOI MOSFET with (001) Ge surface.

***Keywords*—** Electron mobility; Phonon scattering; Germanium; Germanium-on-insulator; MOSFET; Single-gate; Double-gate; Surface orientation.

1. INTRODUCTION

The phonon-limited electron mobility on the (001) Si surface of ultra-thin body (UTB) single-gate (SG) and double-gate (DG) silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) has been widely analyzed [1-5], and its performance merit of high drivability due to the reduction in effective electric field is well known. Recently, electron mobility on the (110) Si surface of SG and DG SOI MOSFETs has been analyzed, and various strain techniques have been proposed and experimentally verified [6, 7]. However, the results yielded by these techniques are not clearly reproducible and fabrication costs are high because strain device fabrication requires new fabrication processes and/or materials. It is suggested that another approach is needed to improve the performance of UTB DG SOI MOSFETs or FinFETs [8].

Esseni et al. published many experimental works targeting electron mobility on the Si (001) surface of UTB SG and DG MOSFETs [9]. DG devices with a sub-10-nm-thick SOI layer

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show a slight improvement in electron mobility at room temperature. However, the influence of surface roughness on the electron mobility of SG and DG devices is complex and has been widely discussed. On this point, theoretical simulation results have been shown recently to explain the behavior of the electron mobility of SG and DG SOI MOSFETs on the (001) Si surface [3]. The influence of surface optical (SO) phonons [10-14] on the electron mobility of the UTB SOI layer was investigated in order to reproduce the measured electron mobility dependence on SOI layer thickness (T_{SOI}) [15]. It was stated that SO phonons and surface roughness scattering contributed to somewhat lower electron mobility than expected. These effects were observed in experiments; however, a conclusive description was not provided because a thorough verification was not possible.

As mentioned previously, FinFETs are frequently fabricated on the (011) Si surface of Si substrates, where the inversion channel is formed on the (111) Si surface [8]. The (111) Si surface has not been well utilized up to now because of its low carrier mobility. However, it is considered that its excellent chemical surface stability is very useful to device fabrication because the fabrication of thin Si devices with (111) surface is very simple as demonstrated in [16, 17]. Thus, creating FinFETs on the (111) Si surface of a (011) Si substrate is not just an abstract discussion. Recently, one-dimensional (1D) self-consistent calculations and relaxation time approximations were performed by our group in order to study the phonon-limited electron mobility of the inversion layer at room temperature for UTB (111) Si layers in SG and DG SOI MOSFETs [18, 19]. Assuming a 5-nm-thick SOI layer, it was shown that intra-valley phonon scattering (acoustic-phonon scattering) in the inversion layer of DG SOI MOSFETs is strongly suppressed over a range of medium effective field values; DG SOI MOSFETs have higher phonon-limited electron mobility than SG SOI MOSFETs. Many simulations strongly suggest that the suppression of acoustic-phonon scattering in a 5-nm-thick DG SOI MOSFET primarily stems from the reduced form factor (F_{00}) value at the lowest subband at medium effective field values.

Ge-based MOSFETs are being extensively studied [20-25] because high electron mobility is attractive for radio-frequency applications [26, 27] and the strain-based mobility-enhancement process has been developed [28-30]. Simplified cross-sectional views of SG and DG germanium-on-insulator (GOI) MOSFETs are shown in Fig. 1. The basic material of GOI substrates for device fabrication is often made by the bonding technology [31]. After adjusting the top germanium film thickness, MOSFETs are fabricated based on the modern device fabrication technology [32]. In many cases, DG MOSFET has a FinFET structure [32] because the double-gate structure is easily realized. In addition, O'regan and Fischetti discussed the impact of remote phonon scattering on the electron mobility of SG GOI MOSFETs with a high-k insulator [33]. They showed that SG GOI MOSFETs keep the electron mobility high at a lower effective field value than SG SOI MOSFETs. Semiconductor industries are now searching new potential businesses and are paying attention to coming space applications. Accordingly, many simulation and modeling studies have been performed [34-38]. However, the radiation hardness [39] and stable performance at low temperature [40-42] demanded for space applications, and semiconductor device physics and technology for future applications must be studied extensively. Simulation studies on the electron mobility of GOI layer are not so extensive [22, 26-28, 33-38]. It is thought that this is because the material property of GOI films is not yet fully mature. Though the Monte Carlo technique was frequently used in prior

simulations [26-28, 33, 36], it consumes too much time to develop appropriate results. In comparison, the self-consistent calculation by the Schroedinger-Poisson-coupled solver is far faster, and the solver basically gives clear interpretation of the phenomenon although it is not easy to implement many scattering mechanisms into simulations [1-3]. At present, however, the industry needs an advanced device technology applicable to space vessels and the next generation of telecommunications; so the material science of Ge-related semiconductors should be further advanced.

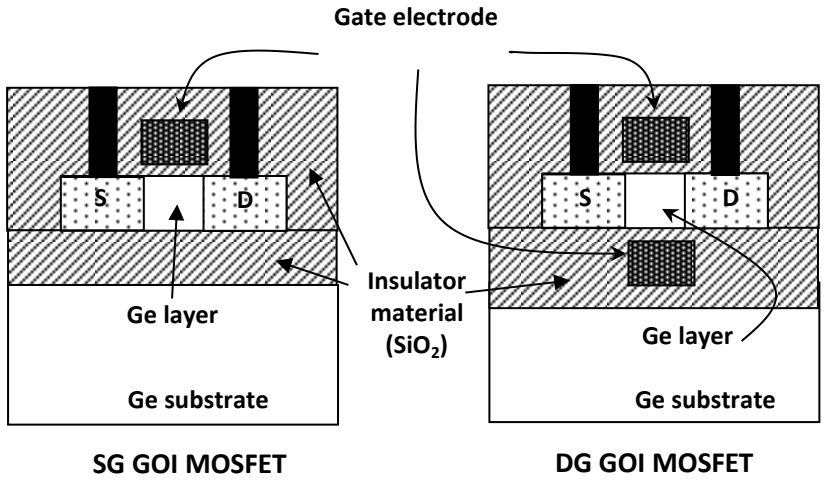

Fig. 1. Simplified cross-sectional views of SG and DG GOI MOSFETs where 'S' denotes the source diffusion region, and 'D' denotes the drain diffusion region.

In this paper, various features of the phonon-limited electron mobility on (001) and (111) Ge surfaces of DG and SG GOI MOSFETs having GOI layer thicknesses (T_{GOI}) ranging from 4 to 30 nm are examined because electron-phonon interaction is always important. Here, it is assumed that acoustic phonons and non-polar optical phonons interact with electrons in the subbands occupied by two-dimensional electrons; intra-subband scattering and inter-subband scattering events are considered. For simplicity, SO phonons are not considered because it is generally considered that their contribution to electron mobility is small [14] provided that the semiconductor layer is not too thin. This paper, accordingly, considers transport in Ge layers thicker than 3 nm. Self-consistent Shroedinger-Posisson-coupled simulation source codes are developed in order to investigate the electron transport characteristics assuming phonon-induced intra-valley and inter-valley scattering processes. Various behaviors of phonon-limited electron mobility of SG GOI MOSFETs and DG GOI MOSFETs are compared. The important features of phonon-limited electron mobility, which depends on materials and device structures, are examined by reviewing the simulation results in detail.

2. SIMULATION MODEL

The simulations assume SG and DG n-channel GOI MOSFETs. It is further assumed that the gate oxide thickness (T_{ox}) of the SG and DG GOI MOSFETs is 3 nm and the buried oxide layer thickness (T_{BOX}) of the SG GOI MOSFET is 200 nm, where the gate oxide and buried oxide layers are made of SiO_2. Impurity concentrations (N_A) in the GOI-layer and Ge

substrate are taken to be $5x10^{15}$ cm^{-3}. Parameters are summarized in Table 1. This paper simulates the phonon-limited electron mobility in the inversion layers of SG and DG GOI MOSFETs on (001) Ge and (111) Ge surfaces at 300 K using a relaxation time approximation based on a 1D self-consistent solution of the Schrödinger and Poisson equations using a non-uniform mesh [43]. Following the lead of other researchers [44-47], the following expression for the relaxation time due to the acoustic phonon scattering process is assumed [44].

$$\tau_{\text{int}\,ra,i}^{-1}(E) = \sum_j \frac{m_{dj} D_{ac}^2 k_B T}{\hbar^3 \rho s^2} F_{ij} u(E - E_j), \tag{1}$$

where D_{ac} is the intra-valley deformation potential for acoustic phonon scattering, m_{dj} is the density-of-state effective mass of electrons in the *j-th* subband, ρ is the silicon's density, s is the longitudinal sound velocity, F_{ij} is the forming factor, and $u(E)$ is the step function. With regard to the deformation potential for acoustic phonon scattering in the Si inversion layer, its anisotropy effect has already been discussed by Fischetti and Laux [14]; they assumed the parabolic band model. It was demonstrated that the magnitude of longitudinal acoustic (LA) phonon scattering is much larger than that of transverse acoustic (TA) phonon scattering [48], that the two-dimensional (2D) anisotropic scattering rate is smaller than that of the 2D isotropic ones [49], and that the impact of non-parabolicity of band structure on the electro-phonon scattering rate is not significant [50]. Accordingly, the isotropic acoustic phonon scattering process and a constant value for the deformation potential are assumed because the aspect of indirect band structure of Ge resembles that of Si. However, in actual calculations of scattering events, the difference in band structure of Ge from that of Si must be taken into account; i.e., electrons occupying the *L* valley interact with those occupying the X valley.

Table 1. Device parameters assumed in the simulations.

Parameters	Materials	Values/units
Gate oxide thickness (T_{ox})	SiO_2	3 nm
Buried oxide thickness (T_{BOX})	SiO_2	200 nm
Doping level of channel region (N_A)	---	$5x10^{15}$ cm^{-3}
Substrate	Ge	---

In Eq. (1), the following approximate expression is used as the forming factor [14].

$$F_{ij} = \int_{-\infty}^{+\infty} |\varsigma_i(z)|^2 |\varsigma_j(z)|^2 \, dz, \tag{2}$$

where $\zeta_i(z)$ is the envelope function revealing aspects of the wave function in the direction parallel to the *z*-axis in this case, and '*i*' indicates the subband label; the integration effectively covers the GOI layer. There have been many discussions on the form factor [14, 51]; its origin is demonstrated in [14]. Since the wave function for the 2D electron gas system includes in-plane off-diagonal factor ($\exp[-iz(w_{13}k_x+w_{23}k_y)/w_{33}]$), where w_{ij} is the reciprocal effective mass and $1/w_{33}= m_z$*[52], we must be careful in calculating the form factor. However, the overlap integral often cancels its in-plane factor because of its complex conjugate nature and the high-barrier well-type potential seen in many cases. The point is whether this is true in the present case or not. This paper assumes the gate/SiO_2/Ge/SiO_2/Ge substrate stack structure shown in Fig. 1 for the SG GOI MOSFET.

The thin Ge layer is surrounded by a high barrier and the wave function is effectively pinned at the SiO_2/Ge interface and finite penetration of the wave function is considered in the following simulations. As a result, it can be anticipated that the off-diagonal factor of the wave function does not significantly influence the form factor. In addition, Uno and Mori [51] recently considered the impact of mechanical mismatch at the SiO_2/Si interface on the form factor; it has been predicted that the mechanical mismatch results in a 15 % reduction in phonon-limited electron mobility in the Si inversion layer compared to the bulk counterpart. In their study, a 25 % reduction in phonon-limited electron mobility in the Ge inversion layer was predicted compared to the bulk counterpart. However, their theoretical expression for the form factor is almost independent of semiconductor layer thickness. It is considered, therefore, that the approximate expression for the form factor is still acceptable for the following consideration of the relaxation time of scattering events [53, 54]. Some additional points will be discussed later again (Figs. 10 and 11 in Section 3.1 and Fig. 19 in Section 3.2).

In addition, the following expression is used for the relaxation time due to the non-polar phonon scattering process.

$$\tau_{\text{int}er,i}^{-1}(E)=\sum_{j}\sum_{r_{ij}}\frac{n_{ij}m_{dj}D_{r_{ij}}^{2}}{\hbar^{2}\rho\omega_{r_{ij}}}F_{ij}$$

$$\times\left\{N_{r_{ij}}\frac{1-f(E+\hbar\omega_{r_{ij}})}{1-f(E)}u(E+\hbar\omega_{r_{ij}}-E_{j})+(N_{r_{ij}}+1)\frac{1-f(E-\hbar\omega_{r_{ij}})}{1-f(E)}u(E-\hbar\omega_{r_{ij}}-E_{j})\right\}, \quad (3)$$

where r_{ij} is the index of phonons yielding inter-valley transition from valley 'i' to valley 'j', n_{ij} is the degeneracy of valley 'j' yielding the inter-valley transition from valley 'i' to valley 'j', D_{rij} is the deformation potential of inter-valley phonons, N_{ij} is the Bose-Einstein distribution function, ω_{rij} is the phonon angular frequency, E_j is the energy offset between two different valleys , and $f(E)$ is the Fermi-Dirac distribution function. In Eq. (3), it is assumed that D_{rij} is a constant value based on the consideration of Fischetti and Laux [14]. Intra-valley nonpolar optical-phonon scattering with transverse optical (TO)-phonons in the X valleys is not taken into account in the following simulations because it is forbidden by symmetry at the zero-th order.

The physical parameters assumed in all simulations are taken from past papers [27, 55, 56] (see Table 2); orientation dependent effective mass values are listed in Table 3 for the Ge (001) surface and in Table 4 for the Ge (111) surface. Electron mobility of the specific *i-th* subband is derived by the following formula:

$$u_i=\frac{q\int(E-E_i)\,\tau_i(E)\,\frac{df}{dE}\,dE}{m_{c,i}\int(E-E_i)\,\frac{df}{dE}dE} \quad (4)$$

where $m_{c,i}$ is the conductivity effective mass of electrons at the specific *i-th* subband, $\tau_i(E)$ is the relaxation time of phonon scattering [1-3, 43], and E_i is the *i-th* subband energy level.

E_{eff} for the SG GOI MOSFET is defined as:

$$E_{eff}=\frac{\int_{Z_0}^{Z_0+T_{GOI}}n(z)E(z)dz}{\int_{Z_0}^{Z_0+T_{GOI}}n(z)dz} \quad (5)$$

where $n(z)$ is the local electron density, $E(z)$ is the local transverse electric field, and z_0 stands for the position of the front semiconductor/insulator interface. On the other hand, E_{eff} for the DG GOI MOSFET is defined as:

$$E_{eff} = \frac{\int_{Z_0}^{Z_0+\frac{T_{GOI}}{2}} n(z)E(z)dz}{\int_{Z_0}^{Z_0+\frac{T_{GOI}}{2}} n(z)dz} \quad (6)$$

Integration is stopped at $T_{GOI}/2$ because we assume a symmetric DG GOI MOSFET.

Table 2. Electronic band parameter values assumed in simulations.

Band parameters for Ge	Values	Units
Energy difference, $\Delta E_{C,(X-L)}$	0.18	eV [56]
Energy difference, $\Delta E_{C,(\Gamma-L)}$	0.14	eV [56]
Free electron mass, m_0	9.11×10^{-31}	Kg [55]
Effective mass, m_{lX}	1.35	m_0 [27, 56]
Effective mass, m_{tX}	0.29	m_0 [27, 56]
Effective mass, m_{lL}	1.59	m_0 [56]
Effective mass, m_{tL}	0.08	m_0 [56]
Effective mass, m_{Γ}	0.04	m_0 [27, 56]
Density, ρ	5320	kg/m^3 [56]
Longitudinal sound velocity, v_l	5400	m/s [56]
Transverse sound velocity, v_t	3200	m/s [56]
Deformation potential, $D_{ac\,\Gamma}$	5.0	eV [27, 56]
Deformation potential, $D_{ac\,L}$	11.0	eV [56]
Deformation potential, $D_{ac\,X}$	9.0	eV [56]
Deformation potential, $(D_tK)_{op\,L}$	5.5	10^8 eV/cm [56]
Optical phonon energy, $\hbar\omega_{op}$	37.04	meV [56]
Inter_{XX} $(D_tK)_{op,\,1}$	0.79	10^8 eV/cm [56]
$\hbar\omega_{op,1}$	8.63	meV [56]
Inter_{XX} $(D_tK)_{op,\,2}$	9.5	10^8 eV/cm [56]
$\hbar\omega_{op,2}$	37.1	meV [56]
Inter_{LL} $(D_tK)_{op,\,1}$	3.0	10^8 eV/cm [56]
$\hbar\omega_{op,1}$	27.6	meV [56]
Inter_{LL} $(D_tK)_{op,\,2}$	0.2	10^8 eV/cm [56]
$\hbar\omega_{op,2}$	10.4	meV [56]
Inter_{LX} $(D_tK)_{op}$	4.1	10^8 eV/cm [56]
$\hbar\omega_{op}$	27.6	meV [56]
$\text{Inter}_{L\Gamma}$ $(D_tK)_{op}$	2.0	10^8 eV/cm [56]
$\hbar\omega_{op}$	27.6	meV [56]
$\text{Inter}_{X\Gamma}$ $(D_tK)_{op}$	10.0	10^8 eV/cm [56]
$\hbar\omega_{op}$	27.6	meV [56]

Table 3. Electron effective mass values in Ge (001) (*L*, *X* and *Γ* bands) assumed in simulations.

	Ge (001) surface [56]			
	L valley	*X* valley (2-fold)	*X* valley (4-fold)	*Γ* valley
m^*_z/m_0 (confinement)	0.117	1.35	0.290	0.040
Conductivity mass/m_0	0.149	0.290	0.477	0.040

Table 4. Electron effective mass values in Ge (111) (*L*, *X* and *Γ* bands) assumed in simulations.

	Ge (111) surface [56]			
	L valley (non-deg.)	*L* valley (3-fold)	*X* valley	*Γ* valley
m^*_z/m_0 (confinement)	1.590	0.090	0.393	0.040
Conductivity mass/m_0	0.080	0.151	0.449	0.040

3. RESULTS AND DISCUSSION

3.1. Electron Mobility on (001) Ge Surface

Given our previous simulation results with regard to thin Si layers [18, 19], it can be expected that a similar phenomenon occurs in a GOI layer on the (001) Ge surface because the conduction band location on the (001) Ge surface resembles that on the (111) Si surface. Self-consistent simulations were performed using the known physical parameters and effective masses for the (001) surface listed in Tables 2 and 3. Note that *X* valleys as well as *L* valleys must be addressed when considering the GOI layer on the (001) Ge surface.

Simulated phonon-limited electron mobility on the (001) Ge surface is shown in Fig. 2 as a function of T_{GOI} for various E_{eff} values; simulated mobility values of the DG and SG GOI MOSFETs are compared. This paper does not show the simulation results of electron mobility for T_{GOI} < 4 nm because ab initio calculations [57] are needed in that range of thickness. It is seen that the DG GOI MOSFET offers superior mobility for T_{GOI} values ranging from 7 to 8 nm in a medium- and high-E_{eff} range. It has been found, through several simulations (not shown here), that maximal mobility enhancement appears around T_{GOI} = 7.2 nm for E_{eff} > ~0.4 MV/cm. However, the expected phonon-limited electron mobility of a 7.2-nm-T_{GOI} DG GOI MOSFET with (001) Ge surface is about 950 $cm^2/V/s$ at E_{eff} = 1 MV/cm. This is about 65% of that of the equivalent DG GOI MOSFET with (111) Ge surface; transport characteristics on the (111) Ge surface are discussed later in detail. In contrast to the Si (111) surface, this indicates that the use of the (001) Ge surface configuration in device applications is not appealing because of the very low mobility. Du et al. showed that the Monte Carlo simulation results of electron mobility in SG GOI MOSFETs with (111) Ge surface are identical to those in SG SOI MOSFETs with (111) Si surface [58]. However, the present simulation results can't be compared with theirs because the DG MOSFET is not assumed [58]. On the other hand, Low et al. studied the performance limits and engineering issues of scaled DG GOI MOSFETs having a sub-5-nm-thick germanium layer [59], but no comprehensive discussion was provided.

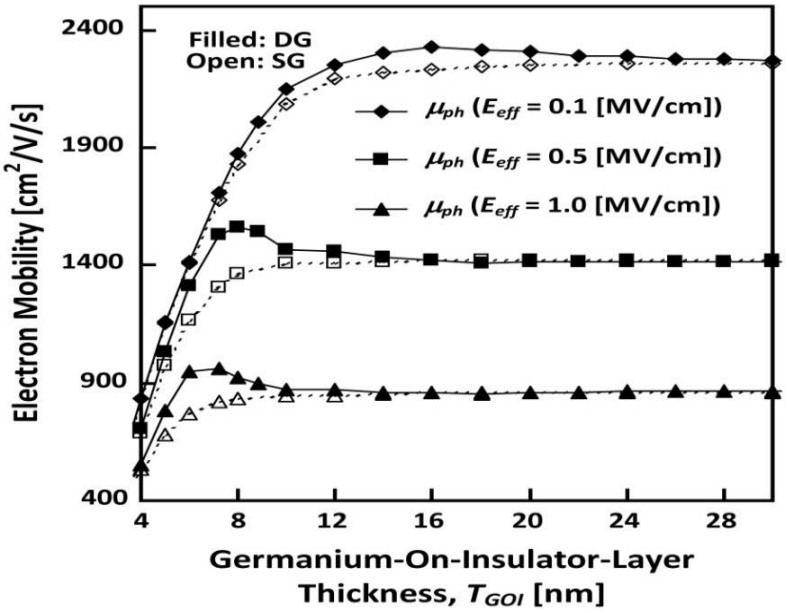

Fig. 2. Simulated phonon-limited electron mobility on the (001) Ge surface as a function of T_{GOI} for various E_{eff} values; simulated mobility values of DG and SG GOI MOSFETs are compared.

Phonon-limited electron mobility on the (001) Ge surface is shown as a function of E_{eff} for DG and SG GOI MOSFETs in Fig. 3; the parameter is T_{GOI}. The electron mobility of the DG GOI MOSFET with 7.2-nm T_{GOI} exceeds that with 10-nm T_{GOI} for E_{eff} > 0.5 MV/cm; in contrast, the SG GOI MOSFET does not exhibit such behavior. As shown in Fig. 3, the DG GOI MOSFET with 7.2-nm T_{GOI} has higher electron mobility than the SG GOI MOSFET for E_{eff} > 0.1 MV/cm. The origin of such electron behaviors in thin Ge layers is quite different from that in thin Si layers because of the difference in conduction band structures; the contribution of electron-acoustic phonon interaction in *X* valley must be accounted for as well as in *L* valley.

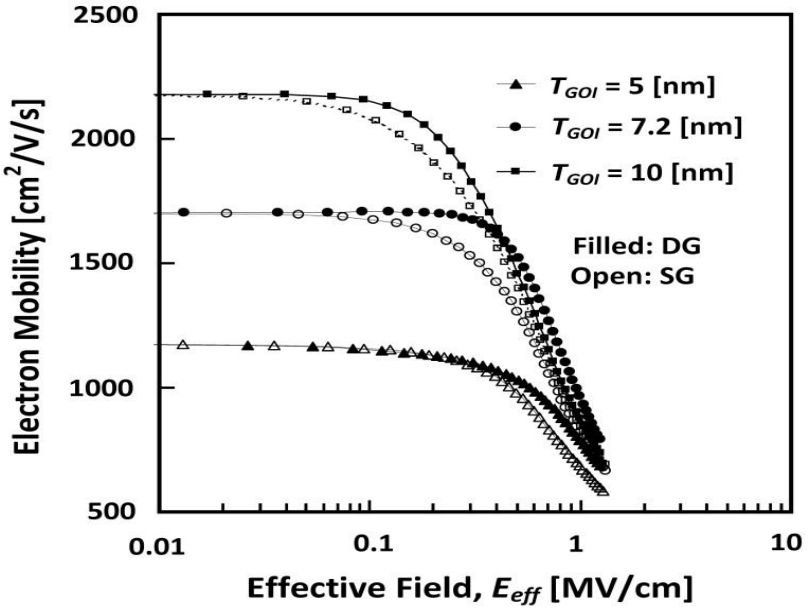

Fig. 3. Simulated phonon-limited electron mobility on the (001) Ge surface as a function of E_{eff} for DG and SG GOI MOSFETs; the parameter is the GOI layer thickness.

Fig. 4 shows the occupation fraction of the lowest subband for *L*, *X* (2-fold and 4-fold), *Γ* valleys as a function of T_{GOI}; Fig. 4(a) for E_{eff} = 0.1 MV/cm and Fig. 4(b) for E_{eff} = 1 MV/cm. It is seen that the occupation fraction of the lowest subband (f_0) of the *L* valley takes maximal value around T_{GOI} = 7 nm regardless of E_{eff} value. At E_{eff} = 1 MV/cm, f_0 of the *L* valley around T_{GOI} = 7 nm is reduced and f_0 of the *X* valley (2-fold) around T_{GOI} = 7 nm increases relative to the case at E_{eff} = 0.1 MV/cm. This is due to the fact that the effective mass in the 2-fold *X* valley is much larger than that in *L* valley. Occupation fraction (f_0) of the *X* valley (2-fold) in the SG GOI MOSFET is higher than that in the DG GOI MOSFET at E_{eff} = 1 MV/cm; this represents a demerit for SG GOI MOSFETs since it implies a high effective mass in the 2-fold *X* valley. It follows that DG GOI MOSFETs should have superior phonon-limited electron mobility to SG GOI MOSFETs in the higher E_{eff} range.

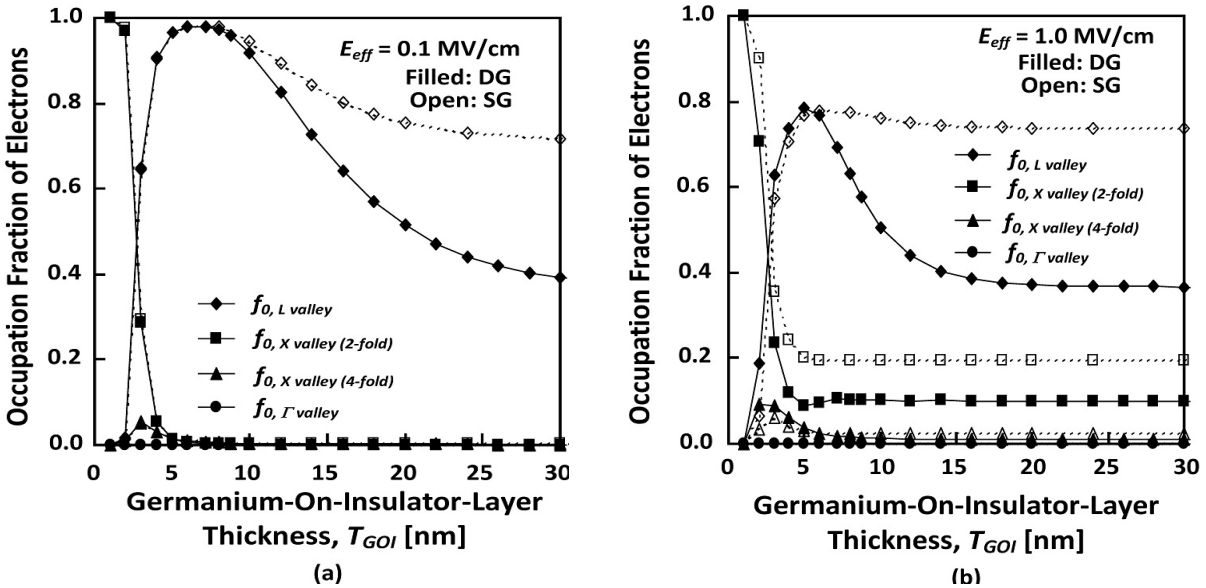

Fig. 4. Occupation fraction of electrons in lowest subband as a function of GOI-layer thickness (T_{GOI}) for *L, X (2-fold and 4-fold)* and *Γ* valleys where (001) Ge surface is assumed: a) low-field condition (E_{eff} = 0.1 MV/cm); b) high-field condition (E_{eff} = 1 MV/cm).

Fig. 5(a) shows the phonon-limited mobility of electrons sharing the lowest subband of the *L* and *X* valleys (2-fold and 4-fold) at E_{eff} = 0.1 MV/cm, and Fig. 5(b) at E_{eff} = 1 MV/cm. Over a wide range of T_{GOI}, the electron mobility of DG GOI MOSFETs is superior to that of SG GOI MOSFETs, although the T_{GOI} value at which the mobility superiority appears to be restricted to a range of small T_{GOI} values when E_{eff} rises. In addition, the *L* valley holds a much higher electron mobility value than the *X* valley except in the sub-5-nm range. The difference in *L*-valley mobility behavior between Figs. 5(a) and 5(b) suggest that the form factor plays an important role in any mobility calculation. A high electric field induces a shift in the peak location of the envelope function $\zeta_i(z)$ toward the surface, which results in an increase in the form factor. With a thinner Ge layer, this requires a higher electric field, as is true for the DG structure. Subsequently, the mobility peak moves to the left in Fig. 5 when E_{eff} increases. It is anticipated that, for electrons sharing the lowest subband, the impact of in-plane wave vector components on the form factor is small because the asymmetric effect of $\zeta_0(z)$ is very limited, where $\zeta_0(z)$ is the envelope function at the lowest subband.

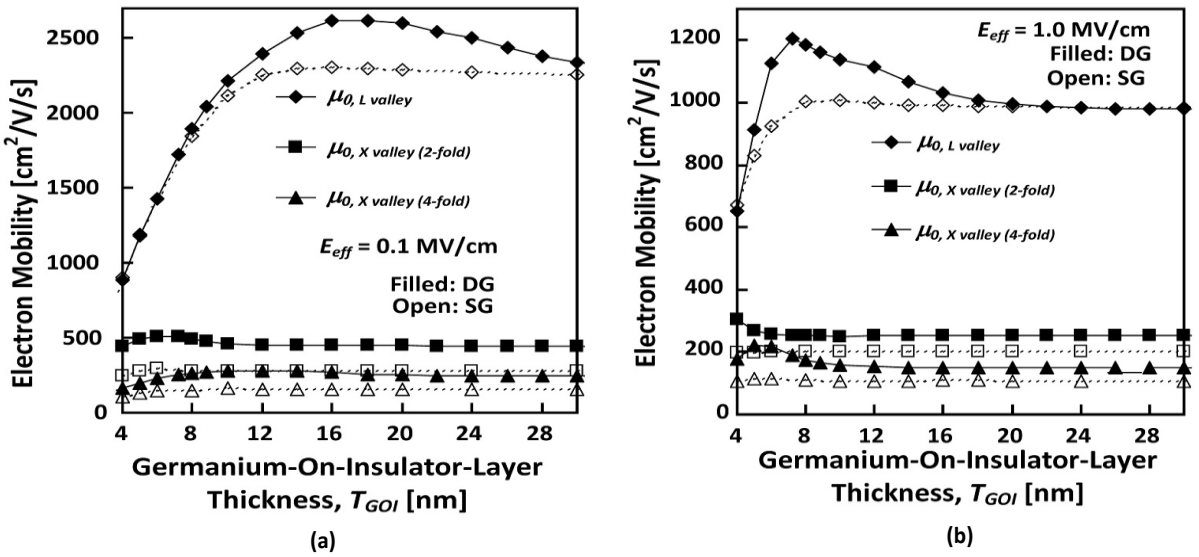

Fig. 5. Simulated phonon-limited mobility of electrons sharing the lowest subband of *L* or *X* valley on the (001) Ge surface as a function of T_{GOI} for various E_{eff} values: a) low-field condition (E_{eff} = 0.1 MV/cm); b) high-field condition (E_{eff} = 1 MV/cm).

Fig. 6 shows the phonon-limited mobility of electrons sharing the lowest subband of a specific valley of a MOSFET having a 7.2-nm-T_{GOI} layer as a function of E_{eff}. It is shown that the phonon-limited electron mobility of the *X* valley of DG GOI MOSFETs is higher than that of SG GOI MOSFETs in a low E_{eff} range, while the phonon-limited electron mobility of the *L* valley of DG GOI MOSFETs is higher than that of SG GOI MOSFETs in medium and high E_{eff} ranges. These aspects of mobility behaviors of electrons sharing the *L* and *X* valleys can be understood by the mechanism described in the above paragraph when the difference in electron effective mass for confinement in the band is taken into account. Fig. 7 shows the occupation fraction (f_n) of electrons sharing the lowest and two higher subbands for the *L* valley of a 7.2-nm-T_{GOI} MOSFET. It is seen that f_0 is almost unity for E_{eff} < 0.5 MV/cm, while f_0 rapidly decreases for E_{eff} > 0.5 MV/cm as E_{eff} increases; the f_0 value of DG MOSFETs is slightly smaller than that of SG MOSFETs because of its flat potential profile in the GOI layer. The high f_0 value for the *L* valley results in a high electron mobility in thin GOI MOSFETs.

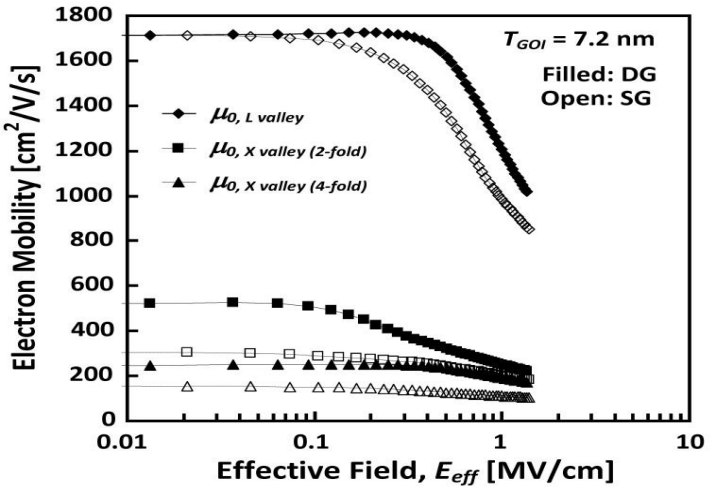

Fig. 6. Simulated phonon-limited mobility of electrons sharing the lowest subband of *L* or *X* valley on the (001) Ge surface as a function of E_{eff} at T_{GOI} of 7.2 nm.

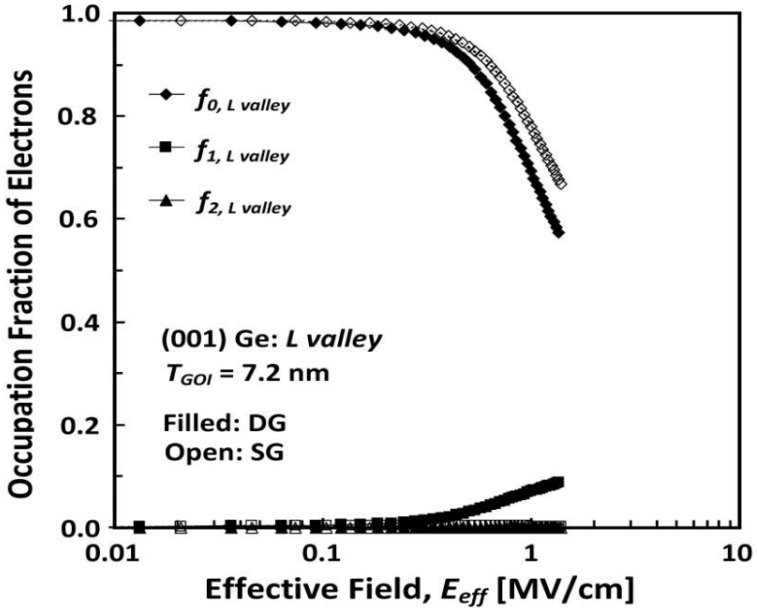

Fig. 7. Simulated occupation fractions (f_0, f_1 and f_2) of electrons sharing the lowest and higher subbands as a function of E_{eff} for the L valley at T_{GOI} of 7.2 nm where (001) Ge surface is assumed.

Hereafter the role of intra-valley phonon scattering and/or inter-valley phonon scattering is discussed on phonon-limited electron mobility of the 7.2-nm-T_{GOI} MOSFET by separately drawing those components in Fig. 8. Fig. 8(a) exhibits the phonon-limited mobility of electrons sharing the lowest subband of the L valley, and Fig. 8(b) does the same for the X valley (2-fold). In Fig. 8(a), $\mu_{0,intra,Lvalley}$ includes both the intra- subband and the inter-subband scattering processes of electrons sharing the lowest subband in the L valley, and $\mu_{0,inter,Lvalley}$ includes the L-valley-to-L-valley and the L-valley-to-X-valley scattering processes of electrons sharing the lowest subband of the L valley. The mobility component of the 4-fold X valley is not shown because its contribution is very limited. In Fig. 8(b), the intra-valley TO-phonon scattering process is not included in the mobility calculation because it is forbidden by band symmetry. In Fig. 8(b), $\mu_{0,intra,Xvalley}$ includes both the intra-subband and the inter-subband scattering processes of electrons sharing the lowest subband in the 2-fold X valley, and $\mu_{0,inter,Xvalley}$ includes the X-valley-to-X-valley and the X-valley-to-L-valley scattering processes of electrons sharing the lowest subband of the 2-fold X valley. It is clearly seen in Fig. 8(a) that the mobility superiority of electrons sharing the L valley of DG GOI MOSFETs for E_{eff} > 0.1 MV/cm is due to the suppression of the intra-valley phonon scattering process, while the inter-valley phonon scattering process is not suppressed in SG GOI MOSFETs. Since the component of inter-valley-phonon-limited electron mobility is still larger than the intra-valley-phonon-limited electron mobility even for E_{eff} > 0.5 MV/cm, the phonon-limited electron mobility is, on the whole, still insensitive to the behavior of the inter-valley-phonon-limited electron mobility component. This is one of the important features of phonon-limited electron mobility in the L valley of thin GOI MOSFETs. In Fig. 8(b), however, the inter-valley-phonon-limited electron mobility component of the 2-fold X valley is smaller than the corresponding intra-valley-phonon-limited electron mobility component. That is, the degradation in inter-valley-phonon-limited electron mobility for E_{eff} > 0.1 MV/cm reduces the entire phonon-limited electron mobility; note that the relative merit of DG GOI MOSFETs holds for E_{eff} < ~0.5 MV/cm because the inter-valley-phonon-limited electron mobility

component of SG GOI MOSFETs is still smaller than that of DG GOI MOSFETs. In a high E_{eff} range (> ~0.5 MV/cm), however, the merit of DG GOI MOSFETs is quite limited as shown in Fig. 8(b) because the difference of mobility values of SG and DG GOI MOSFETs is very small; this also stems from the heavy electron effective mass for conduction and the asymmetric shape of the envelop function $\zeta_0(z)$ of the electrons sharing the lowest subband in SG GOI MOSFETs.

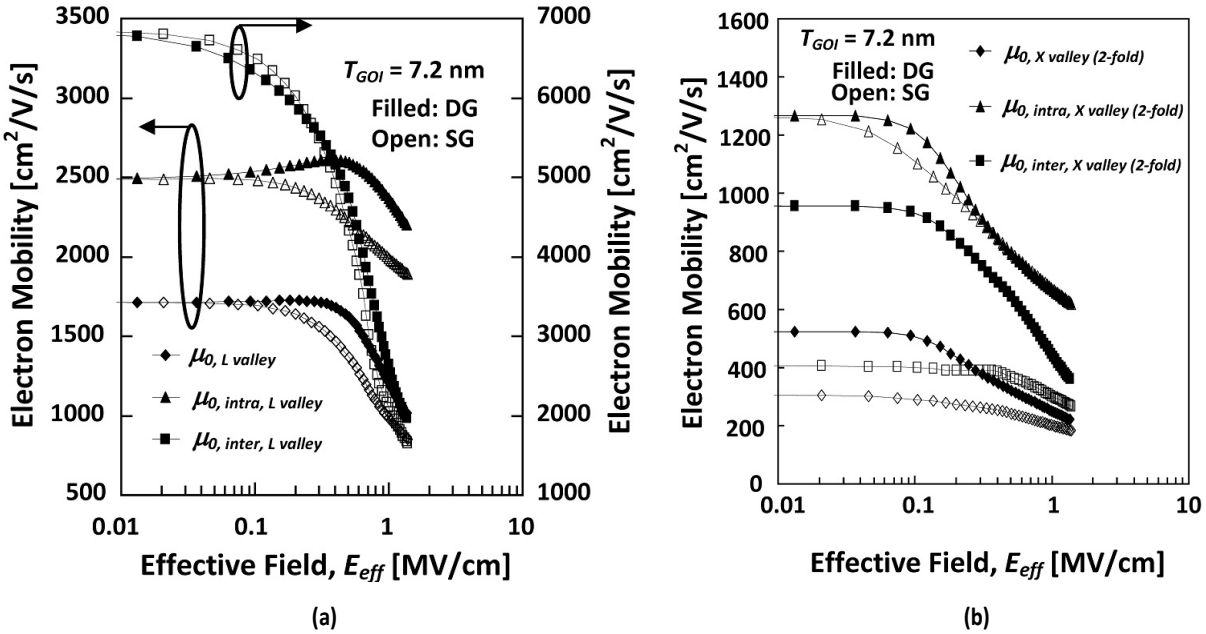

Fig. 8. Intra-valley-phonon-scattering-limited mobility ($\mu_{0,\ intra}$), inter-valley-phonon-scattering-limited mobility ($\mu_{0,inter}$), and overall phonon-limited mobility of electrons sharing the lowest subband of the *L* or *X* valley as a function of E_{eff} for SG and DG GOI MOSFETs with (001) Ge surface channel for T_{GOI} = 7.2 nm: a) *L* valley; b) 2-fold *X* valley.

Moreover, in order to reveal the dominance of the contribution of electrons sharing the lowest subband, the contribution of the mobility of electrons sharing higher subbands is addressed in Fig. 9. Fig. 9(a) shows the mobility components of the *L* valley as a function of E_{eff}, and Fig. 9(b) shows those of the 2-fold *X* valley. Mobility notation in Fig. 9 is the same as that in Fig. 8. Generally speaking, the mobility components of the *L* and *X* valleys are insensitive to E_{eff} for E_{eff} < 2 MV/cm. The primary feature of mobility behavior seen in Fig. 9 is the fact that the inter-valley-phonon-limited mobility is basically smaller than the intra-valley-phonon-limited mobility for electrons sharing the 1st and 2nd exited subbands; this is opposite to the feature seen in Fig. 8. In the case of *L* valley, the difference in phonon-limited mobility is quite small between SG and DG GOI MOSFETs. On the other hand, in the case of *X* valley, the inter-valley-phonon-limited mobility value of DG GOI MOSFETs is higher than that of SG GOI MOSFETs. Since the occupation fractions, f_1 and f_2, are smaller than f_0 as shown in Fig. 7, it is anticipated that the contribution of electrons that share higher subbands is small.

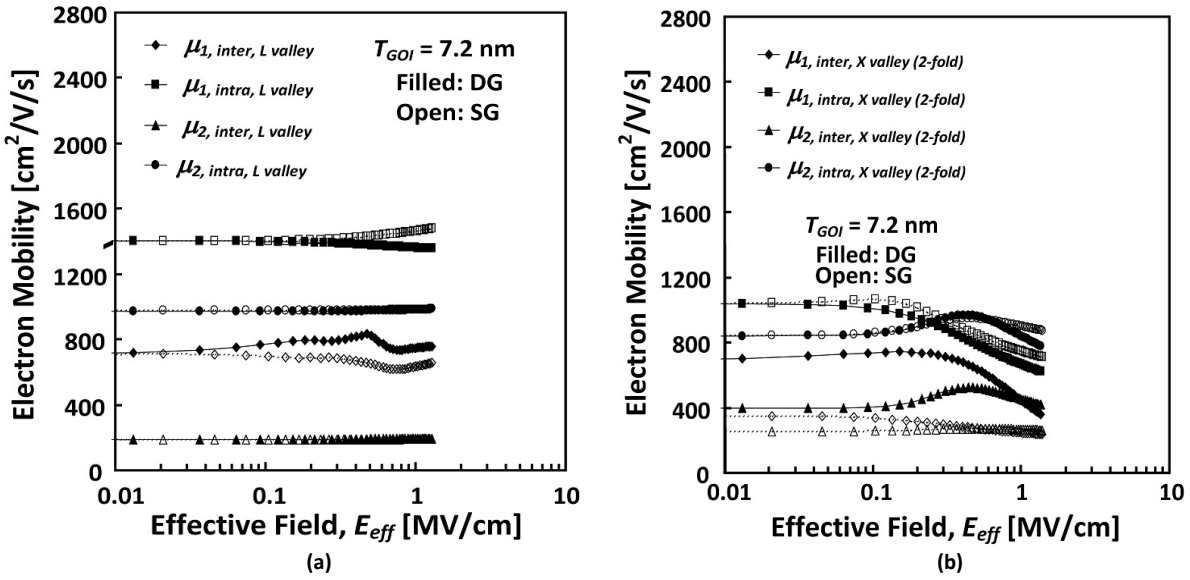

Fig. 9. Intra-valley-phonon-scattering-limited mobility ($\mu_{0,\ intra}$), inter-valley-phonon-scattering-limited mobility ($\mu_{0,inter}$), and overall phonon-limited mobility of electrons sharing the 1st and 2nd excited subbands of the *L* or *X* valley as a function of E_{eff} for SG and DG GOI MOSFETs with (001) Ge surface channel at T_{GOI}= 7.2 nm: a) *L* valley; b) 2-fold *X* valley.

Figs. 10(a) and 10(b) show dependencies of the form factor (F_{ij}) on E_{eff} at T_{GOI} of 7.2 nm for the *L* and 2-fold *X* valleys, respectively. Eq. (2) was assumed in calculating the form factor F_{ij}. As already discussed by Stern and Howard [52], the wave function for the 2D electron gas generally includes off-diagonal contributions. Since the (001) surface orientation of the Ge layer is considered in this section, in the case of *L* valley, some attention to the influence of the off-diagonal factor on the form factor must be paid. However, the recent article by Uno and Mori [51] strongly suggests that the mechanical mismatch at the interface would yield a greater impact on the mobility rather than that factor, so for simplicity we ignore the impact of the off-diagonal factor on the form factor. In Fig. 10(a), F_{00} of DG MOSFETs rapidly decreases as E_{eff} rises for E_{eff} > 0.1 MV/cm, while F_{00} of SG MOSFETs increases as E_{eff} increases for E_{eff} > 0.1 MV/cm. F_{01} of DG MOSFETs is lower by 30 % than F_{00} of DG MOSFETs, which suggests less influence of '*the lowest subband*'-to-'*the 1st excited subband*' inter-subband scattering on the phonon-limited mobility. Though F_{11} and F_{22} values are comparable to the F_{00} value over a wide range of E_{eff}, F_{11} and F_{22} have less impact on the entire phonon-limited electron mobility value because occupation fractions f_1 and f_2 are much smaller than f_0. Since the role of F_{00} is significant in *L* valley, it is expected that intra-subband transition in the lowest subband is dominant. In Fig. 10(b), F_{00} of DG MOSFETs decreases as E_{eff} rises for E_{eff} < 0.1 MV/cm, and it rebounds for E_{eff} > 0.1 MV/cm, while F_{00} of SG MOSFETs straightforwardly increases as E_{eff} increases. F_{01} of DG MOSFETs straightforwardly increases as E_{eff} increases and reaches the F_{00} value, while F_{01} of SG MOSFETs decreases as E_{eff} rises for E_{eff} < 0.1 MV/cm, and it rebounds for E_{eff} > 0.1 MV/cm; however, it holds a much lower value than F_{01} value of DG MOSFETs. As a result, it can be concluded that, in DG MOSFETs, the influence of intra-subband transition (the lowest subband) of electrons sharing *X* band on the phonon-limited mobility is very limited for E_{eff} > 0.1 MV/cm, which is strongly suggested in Figs. 8(b) and 9(b). To show the features of transport in a thin GOI layer, the form factors of

the *L* valley of devices having a 30-nm-thick GOI layer were also simulated as well as those of devices having a 7.2-nm-thick GOI layer.

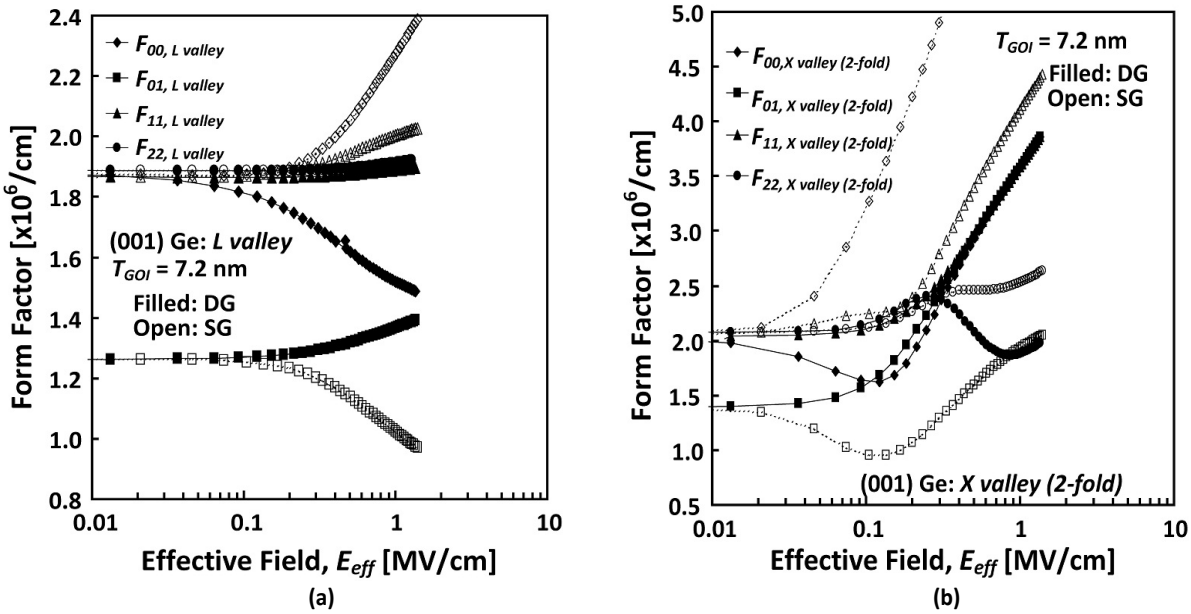

Fig. 10. Simulated form factors (F_{ij}) of electrons sharing the lowest, 1st and 2nd excited subbands of the *L* or *X* valley as a function of E_{eff} for SG and DG GOI MOSFETs with (001) Ge surface channel at T_{GOI} = 7.2 nm: a) *L* valley; b) 2-fold *X* valley.

In Fig. 11, dependencies of the form factor (F_{ij}) on E_{eff} for two T_{GOI} values of 7.2 and 30 nm are shown for the *L* valley. It should be noted that F_{00} of a 7.2-nm-T_{GOI} DG MOSFET decreases as E_{eff} increases for E_{eff} > 0.1 MV/cm, and that F_{00} of a 7.2-nm-T_{GOI} SG MOSFET increases with E_{eff} for E_{eff} > 0.1 MV/cm. On the other hand, it is seen that F_{00} values of a 30-nm-T_{GOI} DG MOSFET and SG MOSFET straightforwardly rise as E_{eff} increases, and that F_{00} of the SG MOSFET is always larger than that of the DG MOSFET.

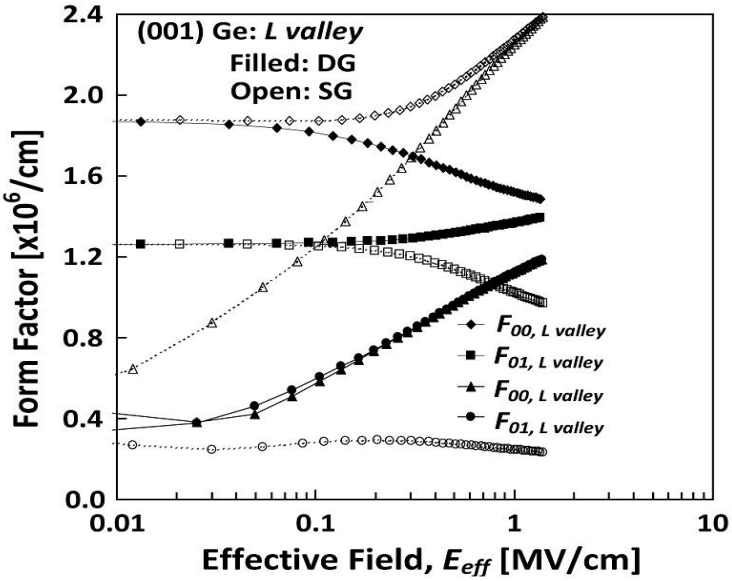

Fig. 11. Simulated form factors (F_{ij}) of electrons sharing the lowest and 1st excited subbands of the *L* or *X* valley as a function of E_{eff} for SG and DG GOI MOSFETs with (001) Ge surface channel for two different T_{GOI} values.

Simulation results of wave functions of electrons of 7.2-nm T_{GOI} MOSFETs at E_{eff} = 0.1 and 1 MV/cm are shown in Figs. 12(a) to 12(d); potential shapes of the GOI layer are also shown to help the consideration. Fig. 12(a) shows those of the *L*-valley electrons of SG MOSFETs, Fig. 12(b) shows those of the *L*-valley electrons of DG MOSFETs, Fig. 12(c) shows those of the 2-fold *X*-valley electrons of SG MOSFETs, and Fig. 12(d) shows those of the 2-fold *X*-valley electrons of DG MOSFETs. It is seen that, at E_{eff} = 1 MV/cm, the *X*-valley electrons of SG and DG MOSFETs offer stronger one-sided or two-sided confinement than the *L*-valley electrons; we anticipate that the uncertainty principle leads to high scattering frequency in the 2-fold *X*-valley. In addition, Ge's permittivity, which is larger than that of Si, must be accounted for. It should be noted that Ge MOSFETs yield a relatively low E_{eff} at the same inversion-layer electron density as Si MOSFETs.

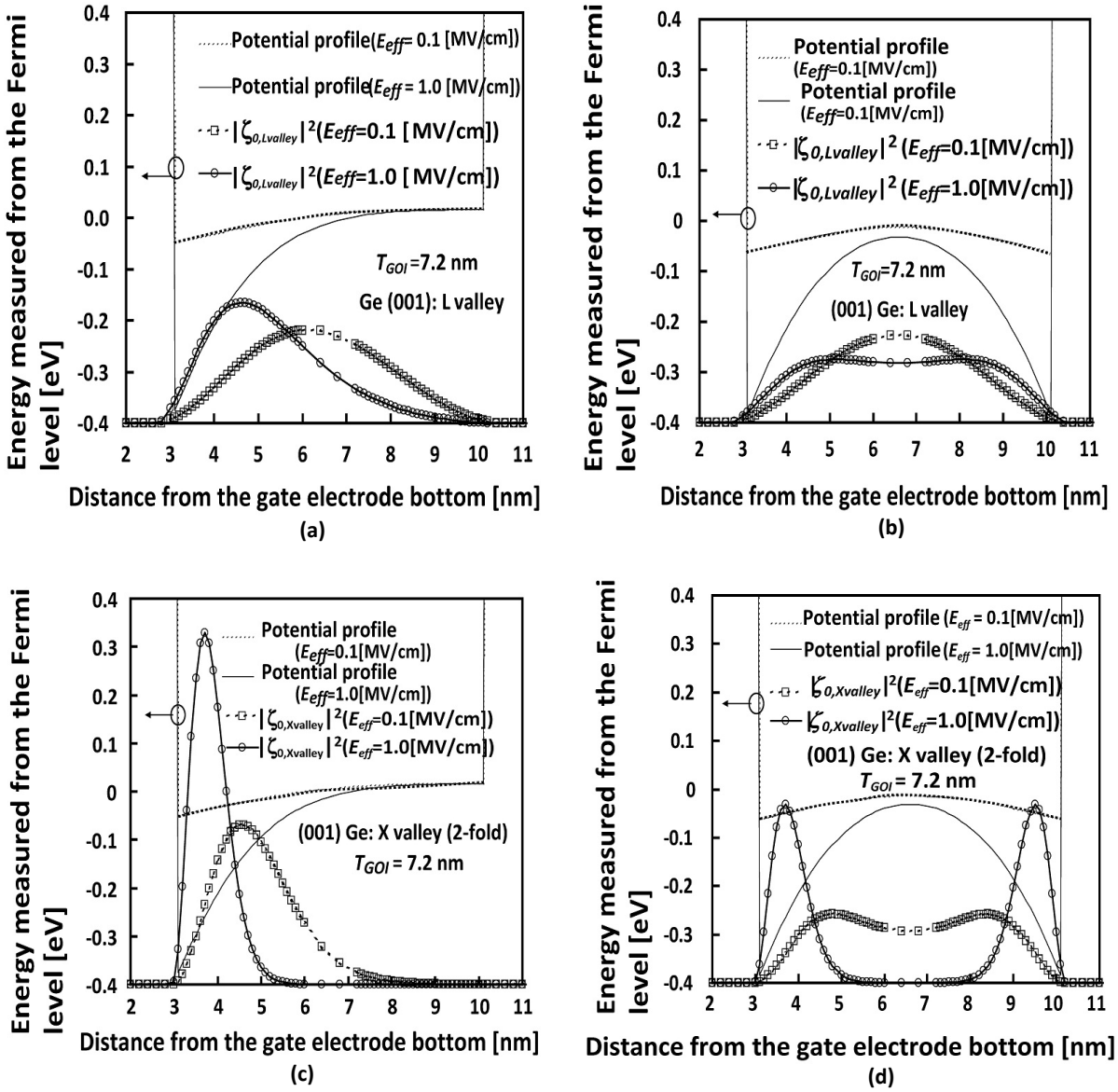

Fig. 12. Simulated profiles of wave functions of electrons sharing the *L* valley and 2-fold *X* valleys for SG and DG GOI MOSFETs with (001) Ge surface channel for two different E_{eff} values at T_{GOI} of 7.2 nm: a) electrons sharing the *L* valley of SG MOSFET; b) electrons sharing the *L* valley of DG MOSFET; c) electrons sharing the 2-fold *X* valley of SG MOSFET; d) electrons sharing the 2-fold *X* valley of DG MOSFET.

3.2. Electron Mobility on (111) Ge Surface

Self-consistent simulations were performed using the known physical parameters and effective masses for the (111) surface listed in Tables 2 and 4; note that the *X* valleys as well as the *L* valleys have to be taken into account for the GOI layer with (111) Ge surface.

Simulated phonon-limited electron mobility on the (111) Ge surface is shown in Fig. 13 as a function of T_{GOI} for various E_{eff} values; simulated mobility values of the DG and SG GOI MOSFETs are compared. In contrast to the (001) Ge surface, it is seen that the SG GOI MOSFET offers superior mobility for T_{GOI} values ranging from 4 to 7 nm in a low to high E_{eff} range. Maximal mobility enhancement appears around T_{GOI} = 4 nm for E_{eff} > 0.1 MV/cm. The expected phonon-limited electron mobility of a 4-nm T_{GOI} SG GOI MOSFET with (111) Ge surface is 2300 cm²/V/s at E_{eff} = 0.5 MV/cm [34, 35]; this is about four times that of the equivalent SG GOI MOSFET with (001) Ge surface. This represents a significant merit of using the (111) Ge surface configuration, rather than the (001) Ge equivalent in device applications. As mentioned in Section 3.1, ab initio calculations are basically necessary in the range of T_{GOI} < 4 nm. Therefore, the apparent merit appearing around T_{GOI} of 4 nm should be verified in future. For DG GOI MOSFET, a slight dip is seen at T_{GOI} of ~ 8 nm for E_{eff} = 0.1 MV/cm. It stems from the partial cancellation of the contribution to the mobility of form factors and occupation fraction of electrons in corresponding subbands.

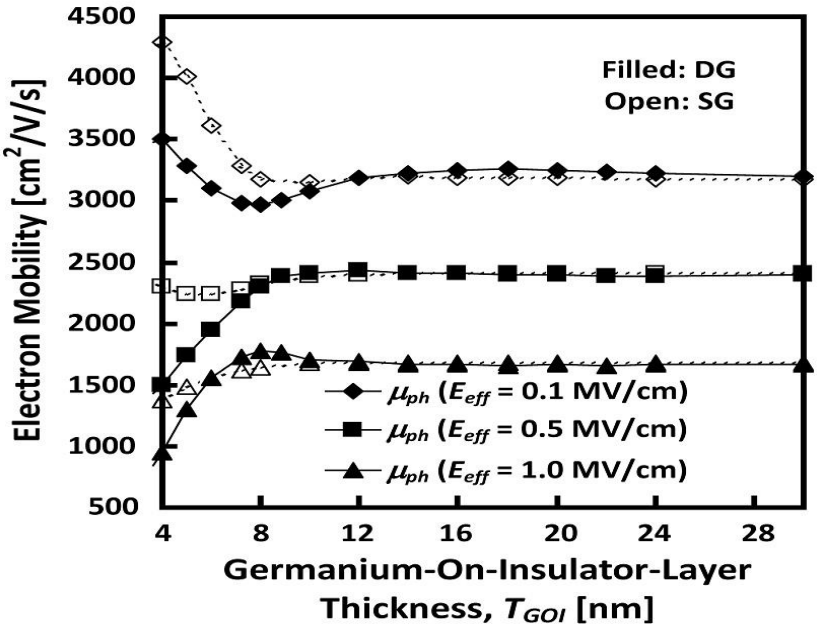

Fig. 13. Simulated phonon-limited electron mobility on the (111) Ge surface as a function of T_{GOI} for various E_{eff} values; simulated mobility values of the DG and SG GOI MOSFETs are compared.

Phonon-limited electron mobility on the (111) Ge surface is shown as a function of E_{eff} for DG and SG GOI MOSFETs in Fig. 14; the parameter is T_{GOI}. The SG GOI MOSFET has higher electron mobility than the DG GOI MOSFET for small T_{GOI} values over a wide range of E_{eff} values; it is expected that the maximal mobility value is obtained around T_{GOI} of 4 nm. However, it should also be noted that phonon-limited electron mobility of SG and DG MOSFETs with a 30-nm-thick GOI layer is comparable to that of a SG MOSFET with a sub-5-nm-thick GOI layer for E_{eff} > 0.2 MV/cm. Therefore, in a practical sense, it can be stated

that using a 5-nm-thick GOI layer is not so meaningful for devices except for its suppression of short-channel effects. In the following, the low-field behavior of the phonon-limited electron mobility of the (111) Ge surface of GOI MOSFETs is focused on.

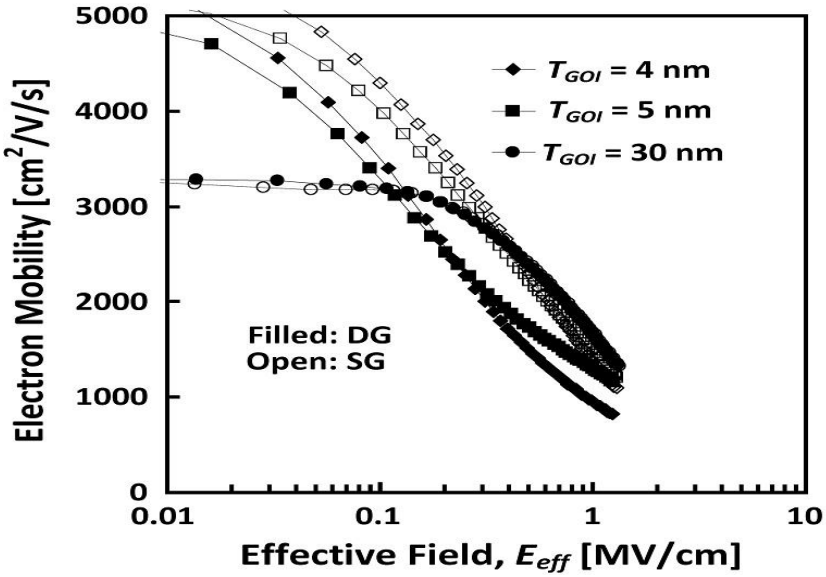

Fig. 14. Simulated phonon-limited electron mobility on the (111) Ge surface as a function of E_{eff} for DG and SG GOI MOSFETs; the parameter is GOI layer thickness.

Fig. 15 shows the phonon-limited electron mobility of the lowest subband for L (non-degenerate and 3-fold) and X valleys as a function of T_{GOI}; Fig. 15(a) for E_{eff} = 0.1 MV/cm and Fig. 15(b) for E_{eff} = 1 MV/cm. As exhibited in Fig. 15(a), the low-field phonon-limited electron mobility of the lowest subband (f_0) of the non-degenerate L valley of SG MOSFETs shows the greatest improvement in mobility at around T_{GOI} = 5 nm, and that the low-field phonon-limited electron mobility of the lowest subband (f_0) of the 3-fold L valley of DG MOSFETs shows that at around T_{GOI} = 20 nm. X-valley electrons have much lower mobility than L-valley electrons because of the heavy conductivity effective mass as shown in Table 4. On the other hand, it can be expected from Fig. 15(b) that the high-field phonon-limited electron mobility of the lowest subband (μ_0) of the non-degenerate L-valley of SG MOSFETs may show the greatest improvement in mobility only for T_{GOI} of sub-5 nm, and it is seen that the high-field phonon-limited electron mobility of the lowest subband (μ_0) of the 3-fold L-valley of DG MOSFETs shows better behavior at around T_{GOI} = 80 nm. Fig. 15 strongly suggests that non-degenerate L-valley electrons are the primary contributor to the low-field high-mobility characteristics of an SG MOSFET with a sub-10-nm T_{GOI} as shown in Figs. 13 and 14.

Fig. 16 shows the occupation fraction of electrons of the lowest subband for L (non-degenerate and 3-fold), X and Γ valleys as a function of T_{GOI}; Fig. 16(a) for E_{eff} = 0.1 MV/cm and Fig. 16(b) for E_{eff} = 1 MV/cm. It is seen in Fig. 16(a) that the occupation fraction of the lowest subband (f_0) of the 3-fold L valley reaches its maximal value at around T_{GOI} = 10 nm, and that the occupation fraction of the lowest subband (f_0) of the non-degenerate L valley reaches its maximal value at T_{GOI} < 4 nm. The f_0 value of the 3-fold L valley is higher than that of the non-degenerate L valley for T_{GOI} > 7 nm at E_{eff} = 0.1 MV/cm, and only a very small difference is seen between SG and DG MOSFETs. On the other hand, it is seen in Fig. 16(b) that the occupation fraction of the lowest subband (f_0) of the 3-fold L valley of SG MOSFETs

remains high for T_{GOI} > 5 nm, and that the occupation fraction of the lowest subband (f_0) of the non-degenerate L valley of SG MOSFETs is higher than that of DG MOSFETs regardless of T_{GOI} value. The occupation fraction of the X valley takes a large value for T_{GOI} < 5 nm. Occupation fraction of the lowest subband level shown here (Fig. 16) and corresponding effective mass value (Table 4) do not provide a simple explanation for the superior electron mobility of SG GOI MOSFETs in a low E_{eff} range, which suggests a complicated contribution of those factors to mobility such as contributions from higher subband electrons. Accordingly, the following considers many factors ruling the phonon-limited electron mobility.

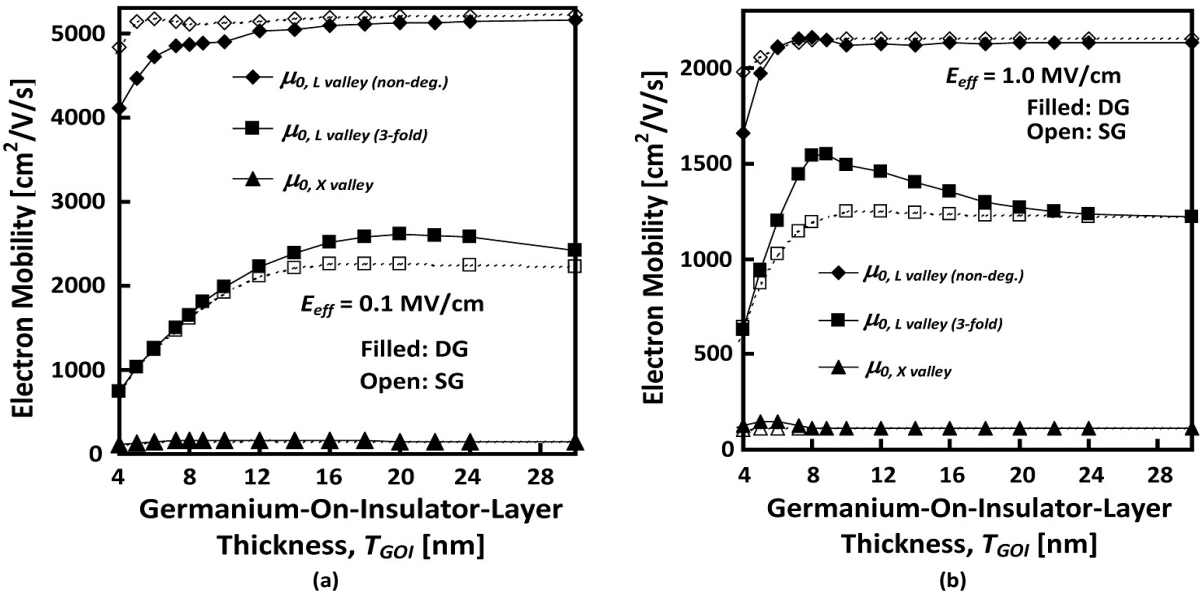

Fig. 15. Simulated phonon-limited mobility of electrons sharing the lowest subband as a function of GOI-layer thickness (T_{GOI}) for L (non-degenerate and 3-fold) and X valleys where (111) Ge surface is assumed: a) low-field condition (E_{eff} = 0.1 MV/cm); b) high-field condition (E_{eff} = 1 MV/cm).

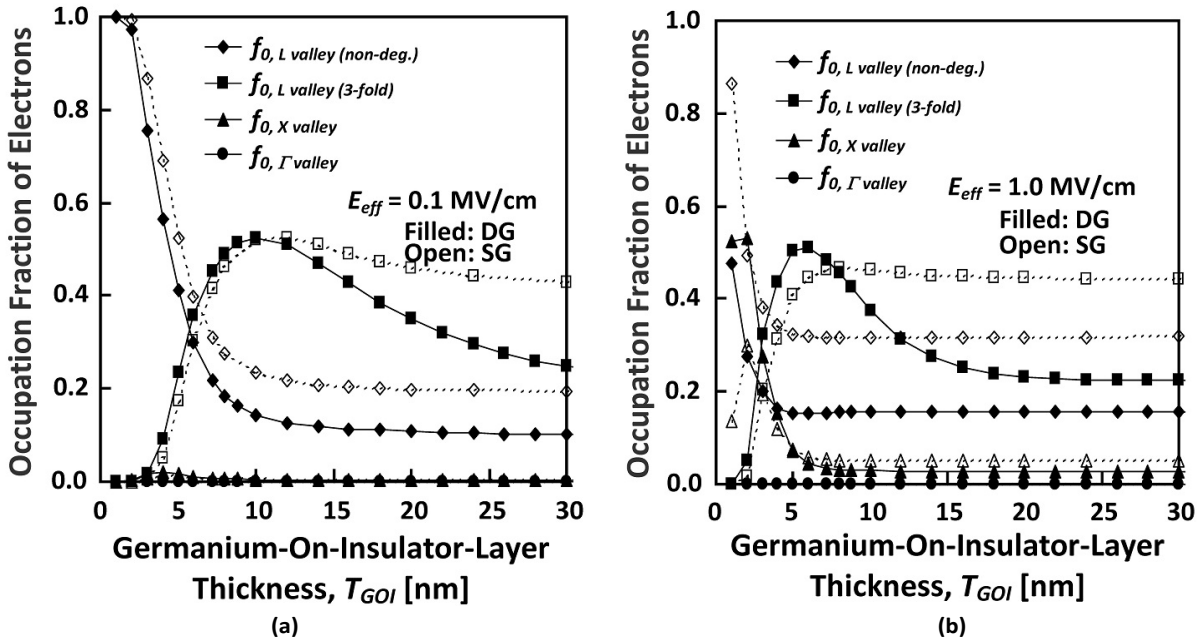

Fig. 16. Simulated occupation fractions of electrons sharing the lowest subband as a function of T_{GOI} for L (non-degenerate and 3-fold), X and Γ valleys on the (111) Ge surface: a) low-field condition (E_{eff} = 0.1 MV/cm); b) high-field condition (E_{eff} = 1 MV/cm).

Figs. 17 to 20 show mobility components of electrons, subband energy levels, and form factors of the non-degenerate *L* valley. Fig. 17 shows the phonon-limited mobility of electrons sharing the lowest subband of the non-degenerate *L* valley as a function of T_{GOI} at E_{eff} = 0.1 MV/cm; intra-valley-scattering-limited mobility ($\mu_{0,intra,Lvalley}$) and inter-valley-scattering-limited mobility ($\mu_{0,inter,Lvalley}$) are separately shown in Fig. 17, where the mobility notations are the same as those in Figs. 8 and 9. $\mu_{0,intra,Lvalley}$ of SG GOI MOSFETs is almost identical to that of DG GOI MOSFETs. On the other hand, $\mu_{0,inter,Lvalley}$ of SG GOI MOSFETs is much higher than that of DG GOI MOSFETs. SG GOI MOSFETs have superior electron mobility compared to DG GOI MOSFETs for T_{GOI} < 10 nm, although the T_{GOI} range at which the superiority appears is restricted when E_{eff} rises (not shown here in detail). It is also suggested from Fig. 17 that intra-valley-phonon-scattering events are the primary determiner of the overall phonon-limited electron mobility behavior.

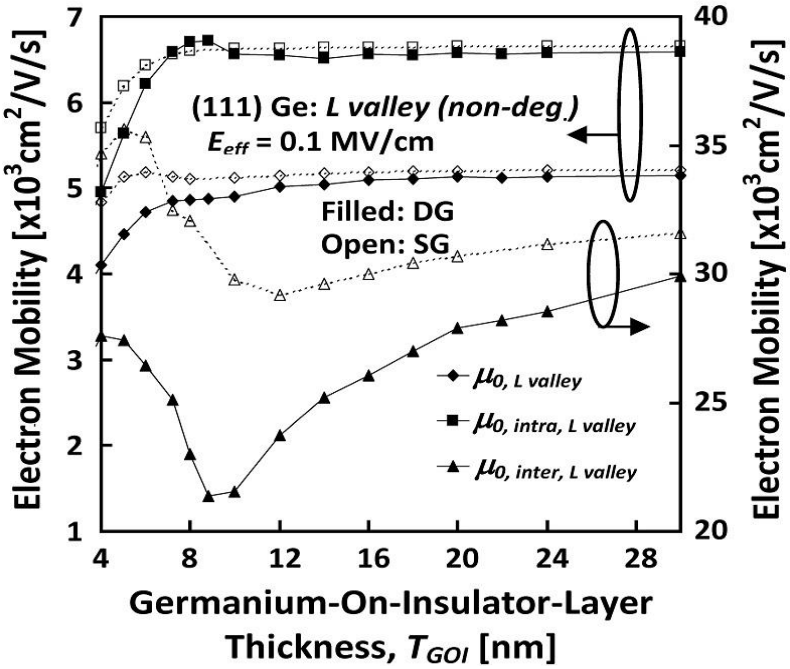

Fig. 17. Simulated phonon-limited mobility of electrons sharing the lowest subband of the non-degenerate *L* valley on the (111) Ge surface as a function of T_{GOI} at E_{eff} = 0.1 MV/cm. $\mu_{0,\ intra,\ Lvalley}$ and $\mu_{0,\ inter,\ Lvalley}$ are also shown separately.

Fig. 18 shows the subband energy levels of the non-degenerate *L* valley as a function of T_{GOI} at E_{eff}= 0.1 MV/cm. E_0 rolls down when T_{GOI} is reduced to the sub-10 nm range. On the other hand, the energy levels of upper subbands (E_1, E_2 and E_3) rise abruptly when T_{GOI} is reduced to the sub-10 nm range. It is anticipated that electrons sharing the lowest subband rule the behavior of the phonon-limited electron mobility of MOSFETs with a sub-10-nm T_{GOI}. These behaviors of subband levels are partially supported by the occupation fraction of the lowest subband shown in Fig. 16(a), but since DG MOSFETs have lower E_0 than SG MOSFETs, further consideration is needed.

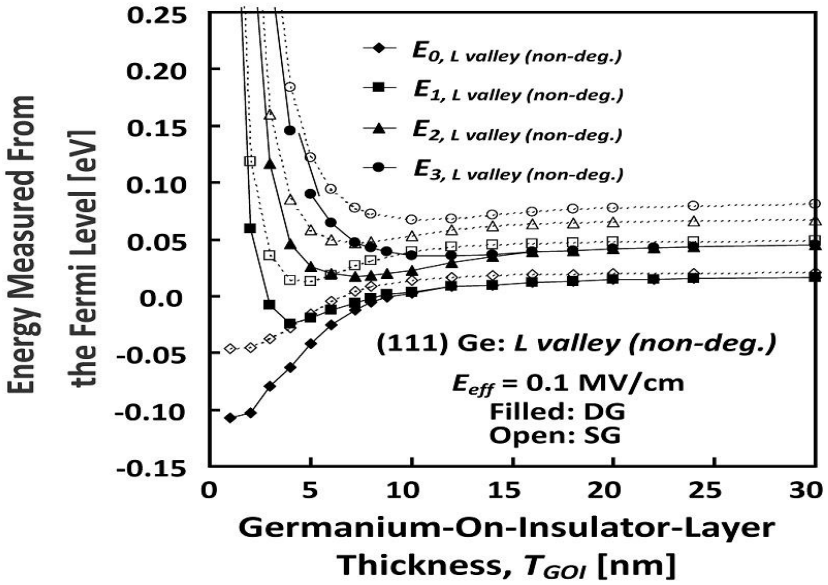

Fig. 18. Simulated subband energy levels (E_0, E_1, E_2, and E_3) measured from the Fermi level as a function of T_{GOI} in the L valley on the (111) Ge surface at E_{eff} = 0.1 MV/cm.

Various form factors (F_{ij}) of electrons sharing the lowest subband of the non-degenerate L valley are shown as a function of T_{GOI} at E_{eff} = 0.1 MV/cm in Fig. 19. It should be noted that F_{00}, F_{01}, F_{11}, and F_{22} of SG and DG MOSFETs rise abruptly in the sub-5-nm T_{GOI} range and F_{00}, F_{11}, and F_{22} have almost identical values, while F_{01} is lower than the other three form factors. Since F_{01} value of SG MOSFETs takes its lowest value among the three other form factors, it is strongly suggested that $\mu_{0,intra,Lvalley}$ is large as seen in Figs. 13, 15(a) and 17 even when F_{00} takes a relatively large value; it is expected that the inter-subband transition (for example, 'i=0' <-> 'j=1') yields no change in wave vector direction, but it does create a small increase in the wave vector of post-transition electrons, in a specific case, which apparently results in a mobility increase. On the other hand, the intra-subband transition (for example, from 'i=0' to 'i=0') always yields a change of wave vector of post-transition electrons, resulting in mobility reduction. These points are discussed in more detail below.

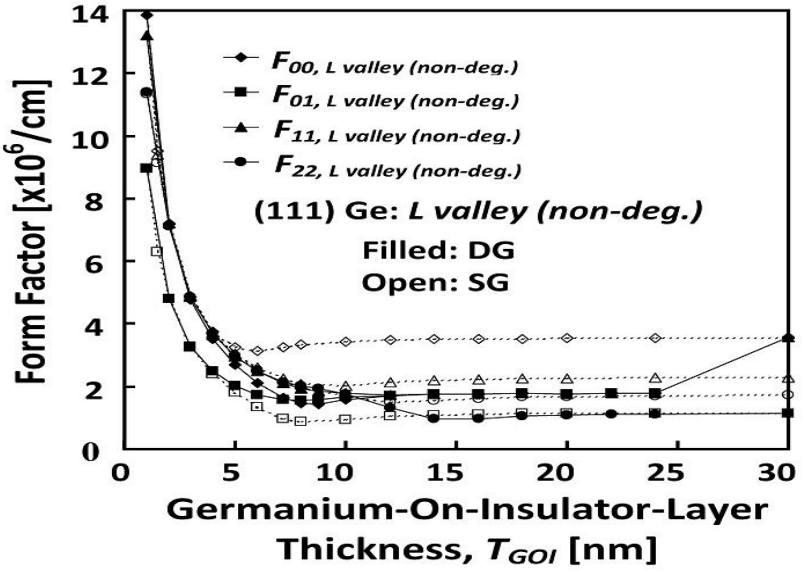

Fig. 19. Simulated form factors (F_{ij}) of electrons sharing the non-degenerate L valley as a function of T_{GOI} for SG and DG GOI MOSFETs with (111) Ge surface channel.

Fig. 20 shows various values of acoustic-phonon-scattering-limited electron mobility of the non-degenerate L valley as a function of T_{GOI} at E_{eff} = 0.1 MV/cm; here, in contrast to Fig. 17, $\mu_{0,intra,Lvalley}$ and $\mu_{0,inter,Lvalley}$ are decomposed into contributions of acoustic-phonon scattering events and optical-phonon scattering events. $\mu_{oo,ac}$ stands for the intra-subband acoustic-phonon-scattering-limited electron mobility at the lowest subband and it is significantly affected by F_{00}. $\mu_{\Sigma 0n,ac}$ stands for the sum of inter-subband acoustic-phonon-scattering-limited electron mobility components (*i.e.* other than $\mu_{oo,ac}$); it reflects to some extent the value of F_{0n}. It is demonstrated that SG MOSFETs have smaller $\mu_{oo,ac}$ than DG MOSFETs. On the other hand, it is clearly revealed that SG MOSFETs have much larger $\mu_{\Sigma 0n,ac}$ than DG MOSFETs. This is a quite interesting result because this phenomenon is not seen in the case of the (001) Ge surface.

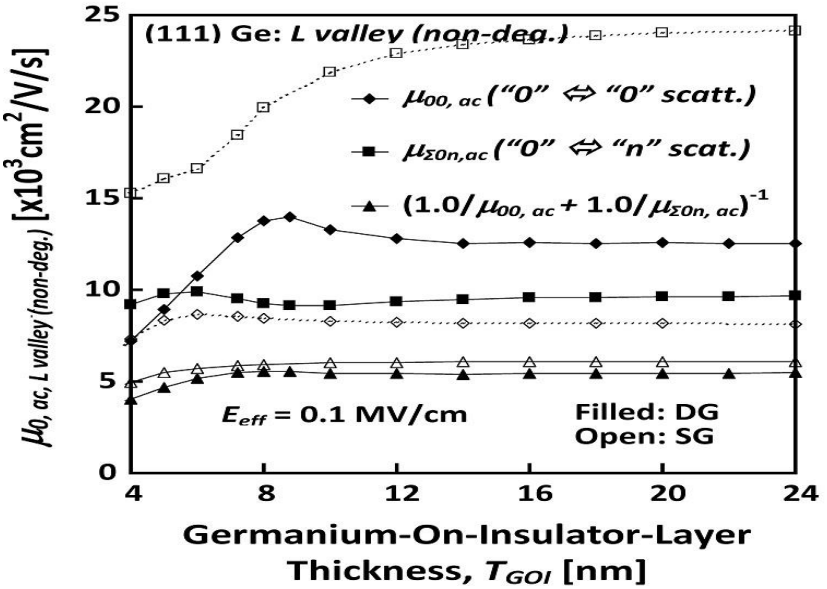

Fig. 20. Simulated acoustic-phonon-limited mobility of electrons sharing the non-degenerate L valley on the (111) Ge surface as a function of T_{GOI} at E_{eff} = 0.1 MV/cm. Components of acoustic-phonon-scattering-limited mobility are shown separately.

In order to pursue deep mechanisms, finally, wave functions of electrons sharing the lowest subband of non-degenerate and 3-fold L valleys are plotted in Fig. 21. As one example, wave functions of electrons are calculated for MOSFETs having a 4-nm T_{GOI} at E_{eff} = 0.1 and 1 MV/cm. Potential shapes of the GOI layer are also shown to help the consideration. Fig. 21(a) shows those of electrons sharing the non-degenerate L-valley of SG MOSFETs, Fig. 21(b) shows those of electrons sharing the non-degenerate L-valley of DG MOSFETs, Fig. 21(c) shows those of electrons sharing the 3-fold L-valley of SG MOSFETs, and Fig. 21(d) shows those of electrons sharing the 3-fold L-valley of DG MOSFETs. Obvious differences can be seen between the wave functions of the non-degenerate and 3-fold L valleys; the distinct difference in the wave functions of inversion layer electrons of SG and DG MOSFETs appears in the non-degenerate L valley, while only a slight difference is seen in case of the 3-fold L valley. In the non-degenerate L valley, at E_{eff} =1 MV/cm, the one-sided or two-sided confinement of electrons is very strong for both SG and DG MOSFETs, which results in a high scattering rate and low mobility, basically because of the uncertainty principle. On the other

hand, at E_{eff} = 0.1 MV/cm, the confinement of electrons is not strong for both SG and DG MOSFETs. Since the occupation fraction of the lowest subband of the non-degenerate L valley is at most 0.5 in the case of T_{GOI} = 4 nm, half the electrons share higher-subbands. Fig. 19 demonstrates that F_{00} is one of the most significant form factors in the low field case. Therefore, it is concluded from Figs. 20 and 21 that the intra-subband scattering process of the lowest subband is not the primary contributor to the high mobility characteristic of the (111) Ge surface; it is suggested that inter-subband scattering processes play an important role.

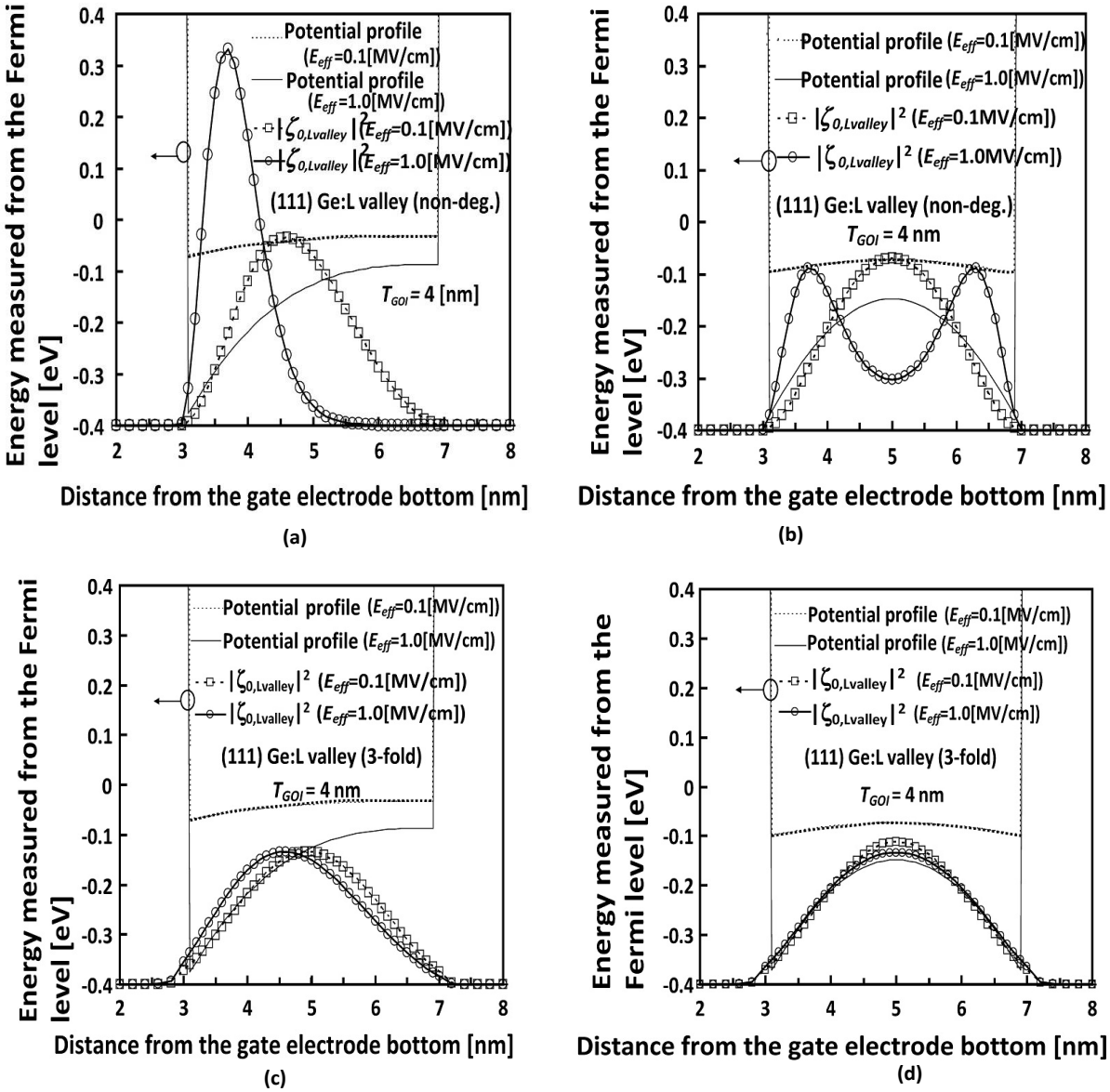

Fig. 21. Simulated profiles of wave functions of electrons sharing the non-degenerate and 3-fold L valleys for SG and DG GOI MOSFETs with (111) Ge surface channel for two different E_{eff} values at T_{GOI} of 4 nm: a) electrons sharing the non-degenerate L valley of SG MOSFET; b) electrons sharing the non-degenerate L valley of DG MOSFET; c) electrons sharing the 3-fold L valley of SG MOSFET; d) electrons sharing the 3-fold L valley of DG MOSFET.

3.3. Progress of Discussion

In the case of MOSFETs with an ultrathin GOI (or SOI) layer, the local-thickness-fluctuation-induced (LTFI) scattering must be considered as well as conventional surface

roughness because the LTFI scattering event cannot be neglected in sub-10-nm-thick layer [46]. The physical model was controversial because no comprehensive fluctuation model has been established based on the local thickness fluctuation. Recently, however, a rigorous surface-roughness scattering model has been proposed [60] and a comprehensive discussion was provided. The article showed that the simulation results of mobility for T_{GOI} < 4 nm are not reliable when the surface-roughness scattering process is not included in the simulation. In addition, the first-principle approach to SOI and GOI structures demonstrates the dependence of the effective mass on layer thickness [61]. The study suggests that the electron mobility of the GOI layer must be reconsidered for layers under 10-nm thickness. Therefore, this article does not show simulation results of mobility for T_{GOI} < 4 nm.

The acoustic-phonon confinement effect has recently been studied [62] for the Si layer because the conventional matrix element of phonon scattering has been calculated assuming the bulk phonon mode. It has been shown that confined acoustic-phonons enhance the scattering, and that they degrade the phonon-limited electron mobility by about 30 % in the SOI layer thickness range of 5-10 nm [49]; we note that the surface orientation dependence of the acoustic phonon confinement was not considered, so its quantitative influence remains unclear.

It has been suggested, for the SOI layer, that the surface optical (SO) phonon mode [3, 10-14] degrades electron mobility when a high-*k* gate insulator is used because of the large difference between the static and the optical permittivities of high-*k* gate insulators [10-14]. It is estimated that SO phonons primarily assist inter-subband transitions in the SOI layer thickness range of sub-5-nm. As described previously, no simulation results of mobility for T_{GOI} < 4 nm are shown in this paper.

Systematic experimental results on electron mobility on the Ge surface are very limited. Recent experimental results on the electron mobility of GOI MOSFETs demonstrate that the electron mobility on the (001) surface is not so sensitive to the GOI layer thickness (T_{GOI}) from 60 nm to 20 nm [21]. This basically matches the simulation results shown in Fig. 2. Monte Carlo simulations [27] and simplified self-consistent simulation results [34] demonstrate that the phonon-limited electron mobility on the Ge surface of the GOI layer depends on T_{GOI} and E_{eff}. In [34], simulation results corresponding to Figs. 2, 3, 13, and 14 are briefly demonstrated. Though they apparently reveal mobility behaviors similar to those shown in Figs. 2, 3, 13 and 14, the present simulation results cannot be compared with them because the simulations in [34] don't take account of inter-band scattering.

As described above, some recent papers suggest the necessity of further study on the impact of phonon scattering events on carrier mobility; this suggests that the present simulation results of electron mobility are somewhat overestimated quantitatively. However, it is thought that the present prediction still remains meaningful because this article discussed the fundamental aspects of phonon-limited electron mobility. In addition, as already mentioned, many companies are now paying attention to future space applications. High performance at low-temperatures [40-42] and radiation hardness [39] are strongly requested for spacecrafts and satellites. In this sense, it is very noteworthy that this paper has predicted that GOI MOSFETs fabricated on a chemically stable surface should show high performance.

4. CONCLUSIONS

This paper has demonstrated one-dimensional self-consistent simulation results based on relaxation time approximations of the phonon-limited electron mobility of the inversion layer at room temperature for ultra-thin body (001) Ge and (111) Ge layers in SG and DG GOI MOSFETs. Assuming a 7.2-nm-thick GOI layer on the (001) Ge surface, it has been demonstrated that intra-valley phonon scattering in the DG GOI MOSFET inversion layer is strongly suppressed within a range of medium and high E_{eff} values; DG GOI MOSFETs have higher phonon-limited electron mobility than SG GOI MOSFETs. Many simulations strongly suggested that the suppression of intra-valley-phonon scattering in a 7.2-nm-thick DG GOI MOSFET primarily stems from the reduction in the form factor at medium and high E_{eff} values. However, it is considered that the use of the (001) Ge surface in DG GOI MOSFETs offers little merit because the difference in mobility values of SG and DG GOI MOSFETs is small in a range of high E_{eff} values. In other words, the use of the (001) Ge surface in DG GOI MOSFETs offers a great merit for low-voltage applications that are required in sensor networks.

It has also been demonstrated that the superior electron mobility of SG GOI MOSFETs with (111) Ge surface indicates a great merit of this structure with regard to radio-frequency applications because inter-subband acoustic-phonon scattering events are significantly reduced in the non-degenerate L valley. The primary mechanism responsible for this is that some inter-subband form factors (such as F_{01}) of electrons sharing the lowest subband of the non-degenerate L valley decrease at low E_{eff} values, while the intra-subband form factor (F_{00}) of electrons sharing the lowest subband of the non-degenerate L valley holds a large value. The expected phonon-limited electron mobility of a 4-nm T_{GOI} SG GOI MOSFET, for example, with (111) Ge surface, is about 2300 $cm^2/V/s/$ at E_{eff} = 0.5 MV/cm; this is about four times that of the equivalent SG GOI MOSFET with (001) Ge surface. However, it is anticipated that ab initio calculations are necessary for T_{GOI} < 4 nm. Therefore, the apparent merit appearing around T_{GOI} of 4 nm should be verified in the future.

Though the simulation results demonstrated in this paper should be examined in detail from the viewpoints of device fabrication engineering, they suggest that the SG GOI MOSFET with (111) Ge surface has better potential for future radio-frequency applications and space applications because the chemical stability of the (111) surface of Ge is very important with regard to device reliability.

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